

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-25 (cancelled).

Claim 26 (new): An active termination circuit mounted in a memory circuit, and comprising:

- a termination resistor; and

- a control circuit which receives an externally supplied active termination control signal, and which selectively switches on and off the termination resistor in response to the active termination control signal;

wherein said control circuit comprises a first signal path for synchronizing the active termination control signal and a second signal path for asynchronously propagating the active termination control signal, and a switching circuit which selectively outputs a signal of the first or second signal paths, and wherein the output of the switching circuit controls an on/off state of the termination resistor.

Claim 27 (new): An active termination circuit as claimed in claim 26, wherein the switching circuit is responsive to an operational mode signal to selectively output the signal of the first or second signal paths.

Claim 28 (new): An active termination circuit mounted in a memory circuit, and comprising:

- a termination resistor which provides a termination resistance for the memory circuit; and

- a control circuit which receives an externally supplied active termination control signal, and which is responsive to an operational mode of the memory circuit

to selectively synchronously or asynchronously switch on and off the termination resistor according to the active termination control signal.

Claim 29 (new): The active termination circuit as claimed in claim 28, wherein the control circuit synchronously switches on and off the termination resistor according to the active termination control signal when the memory circuit is in an active operational mode, and wherein the control circuit asynchronously switches on and off the termination resistor according to the active termination control signal when the memory circuit is in a standby or power-down operational mode.